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Amendments to the Claims

1. (currently amended): A semiconductor ESD structure comprising:

a semiconductor substrate of a first conductivity type having a first region of a second conductivity type and a first dopant concentration;

a buried region of the second conductivity type formed in the first region;

a second region of the first conductivity type formed in the first region and contacting the buried layer;

a third region of the first conductivity type formed in the first region and contacting the buried layer;

a first isolation region formed in the first region between the second and third regions, wherein the second and third regions and first isolation region form concentric rings in the first region;

a first pair of oppositely doped regions formed in the second region; and

a second pair of oppositely doped regions formed in the third region.

Claim 2 (cancelled).

3. (original): The structure of claim 1 wherein the first isolation region comprises a diffused region having a second dopant concentration greater than the first dopant concentration.

4. (original): The structure of claim 3 wherein the first isolation region has a surface dopant concentration of greater than about 1.0×10^{18} atoms/cm³.

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5. (original): The structure of claim 1 wherein the first isolation region extends through the first region and contacts the buried region.
6. (original): The structure of claim 1 wherein the first region comprises an epitaxial layer.
7. (original): The structure of claim 1 wherein the first pair of oppositely doped regions are shorted together.
8. (original): The structure of claim 1 wherein the second pair of oppositely doped regions are shorted together.
9. (original): The structure of claim 1 further comprising:
a second isolation region formed in the first region adjacent the second region; and
a third isolation region formed in the first region adjacent the third region.
10. (original): The structure of claim 9 wherein the second and third isolation regions extend to the buried region.
11. (original): The structure of claim 1 wherein one region of the first pair of oppositely doped regions has a resistance that is about twice that of the other region in the first pair.
12. (original): The structure of claim 1 wherein one region in the second pair of oppositely doped regions has a resistance that is about twice that of the other region in the second pair.
13. (currently amended): The structure of claim 1 further comprising a fourth isolation region formed in the

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first region and surrounding the buried region, the second and third regions, and the first isolation region.

14. (original): The structure of claim 1 wherein the buried region, the second region, and the third region form a temperature compensated device.

15. (original): The structure of claim 1 wherein the buried region and the second region form a buried avalanche region.

16. (original): The structure of claim 1 wherein the buried region and the third region form a buried avalanche region.

17. (original): The structure of claim 1 whereon one of the first pair of oppositely doped regions and the second pair of oppositely doped regions is shorted together to provide a reduced capacitance device.

18. (original): The structure of claim 1 wherein the buried region and the second region generate a V_{BE} voltage and the buried region and the third region generate an avalanche voltage during an ESD trigger event.

19. (original): The structure of claim 1 wherein the buried region and the third region generate a V_{BE} voltage and the buried region and the second region generate an avalanche voltage during an ESD trigger event.

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20. (original): A semiconductor device comprising:
a first ring region of a first conductivity type formed in a layer semiconductor material of a second conductivity type and having a first doping concentration;
a second ring region of the first conductivity type formed in the layer of semiconductor material;
a first doped region of the second conductivity type within the layer of semiconductor material and coupled to the first and second ring regions; and
a third ring region comprising an isolation region between the first and second ring regions.
21. (original): The device of claim 20 wherein the third ring contacts the first doped region.
22. (original): The device of claim 20 further comprising:
a second doped region of the first conductivity type formed in the first ring; and
a third doped region of the second conductivity type formed in the first ring.
23. (original): The device of claim 22 further comprising:
a fourth doped region of the first conductivity type formed in the second ring region; and
a fifth doped region of the second conductivity type formed in the second ring region.
24. (original): The device of claim 20 further comprising:
a first contact structure coupled to the first ring region; and
a second contact structure coupled to the second ring region.

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25. (original): The device of claim 24 wherein one of the first and second contact structures includes a polycrystalline semiconductor material.

26. (original): The device of claim 20 wherein the first doped region comprises a buried region.

27. (original): The device of claim 20 further comprising a fourth ring region comprising an isolation region formed in the layer of semiconductor material adjacent the first ring region and contacting the first doped region.

28. (original): The device of claim 20 further comprising a fifth region comprising an isolation region formed in the layer of semiconductor material adjacent the second ring region and contacting the first doped region.

29. (original): The device of claim 20 wherein the first, second, and third ring regions are substantially concentric.

30. (original): The device of claim 20 wherein the third ring region comprises a diffused region having a second dopant concentration greater than the first dopant concentration.

31. (original): The device of claim 20 wherein one of the third ring region, fourth ring region, and fifth ring region comprises a passivated trench.

Claims 32-38 (cancelled).